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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,777	03/04/2004	Michikazu Matsumoto	60188-793	4422

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,777	MATSUMOTO, MICHIKAZU	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-18 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-18* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the election filed December 19, 2005.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Election/Restrictions

4. Applicant's election of Embodiment XIII in the reply filed on 12/19/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "the dummy pattern is either a pattern made of a dummy gate electrode" (See Claim 17). Merriam-Webster defines either as being the one or other of two. However, Applicant has not disclosed more than one item.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 14, 15 and 17, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (U.S. Patent No. 6,110,771) in view of Matsuoka et al. (U.S. Patent No. 6,333,541) and Shepela et al. (U.S. Patent No. 6,060,397).

In regards to claim 14, Ahn discloses the following:

a) a MOS transistor with a plurality of gate electrodes (124a and 124b) (For Example: See Figure 3);

b) the gate electrodes are formed on a semiconductor substrate (121) having a silicon layer at least in the surface thereof (For Example: See Figure 3);

c) the MOS transistor is formed in an element region surrounded with an isolation insulating film (122) (For Example: See Figure 3);

d) the gate electrodes are arranged between the other gate electrodes or between one of the other electrodes and a dummy pattern (124c and 124d) with a space left from each side thereof (For Example: See Figure 3);

e) sidewalls (125are provided on side walls of each of the gate electrodes and on side walls of another said gate electrode (For Example: See Figure 3);

f) a first silicide layer (128) is formed in the upper portion of the gate electrode (For Example: See Figure 3);

g) a second silicide layer (128) is formed in a portion of the semiconductor substrate surface which is located in part of the element region between the gate electrode and at least one of another gate electrode and the dummy pattern (For Example: See Figure 3).

In regards to claim 14, Ahn fails to disclose the following:

a) the gate length of .15 um.

However, Matsuoka et al. ("Matsuoka") discloses a gate length of .15 um (For Example: See Column 1 Lines 14 and 15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Ahn to include a gate length of .15 um as disclosed in Matsuoka because it aids in helping the device run faster (For Example: See Column 1 Lines 10-23).

Additionally, since Ahn and Matsuoka are both from the same field of endeavor, the purpose disclosed by Matsuoka would have been recognized in the pertinent art of Ahn.

b) the first silicide layer has a greater thickness than the second silicide layer.

However, Shepela et al. ("Shepela") discloses a first silicide layer (10) has a greater thickness than the second silicide layer (7) (For Example: See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Ahn to include a first silicide layer having a greater thickness than the second silicide layer as disclosed in Shepela because it aids in providing low sheet resistance (For Example: See Column 2 Lines 13-20).

Additionally, since Ahn and Shepela are both from the same field of endeavor, the purpose disclosed by Shepela would have been recognized in the pertinent art of Ahn.

In regards to claim 15, Ahn discloses the following:

a) the dummy pattern is a dummy gate electrode pattern having the shape of a gate electrode which is an electrode pattern having the shape of a gate electrode and the dummy pattern is an electrode which is not electrically connected to a semiconductor integrated circuit of the semiconductor device (For Example: See Figure 3 and Column 3 Lines 52-59).

In regards to claim 17, Ahn discloses the following:

a) a dummy gate electrode pattern which is an electrode pattern having the shape of a gate electrode with side walls of the dummy pattern provided with side walls of the dummy pattern provided with sidewalls and is not electrically connected to a semiconductor integrated circuit of the semiconductor device (For Example: See Figure 3 and Column 3 Lines 52-59).

9. Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (U.S. Patent No. 6,110,771) in view of Matsuoka et al. (U.S. Patent No. 6,333,541), Shepela et al. (U.S. Patent No. 6,060,397) and Inumiya et al. (U.S. Patent No. 6,251,763).

In regards to claim 16, Ahn fails to disclose the following:

a) a dummy pattern is made of insulating material.

However, Inumiya et al. ("Inumiya") discloses a dummy pattern made of insulating material (For Example: See Column 11 Line 18). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Ahn to include a dummy pattern made of insulating material as disclosed in Inumiya because it aids in preventing deterioration of the reliability of the transistor (For Example: See Column 7 Lines 10-39).

Additionally, since Ahn and Inumiya are both from the same field of endeavor, the purpose disclosed by Inumiya would have been recognized in the pertinent art of Ahn.

In regards to claim 18, Ahn discloses the following:

a) the dummy pattern is formed on the isolation insulating film (For Example: See Figure 3).

Allowable Subject Matter

10. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

February 20, 2006